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10/826,725	04/15/2004	Chun Hsiang Lai	JCLA6643-D	1368

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,725	LAI ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6 and 8-11* is/are rejected.

7)☒ Claim(s) *7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/801,350.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 5 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 13, 15 of copending Application No. 09801350. Although the conflicting claims are not identical, they are not patentably distinct from each other because applicant's [10/826,725] claim 5 is a combination of the copending application [09/801,350] claims 1, 3 and 4.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

1. Claim 10 is objected to because of the following informalities:

Claim 10, lines 6 and 8, "the PMOS transistor" should be "the NMOS transistor". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, Patent No. 5,869,873, in view of Yu, Patent No. 6,031,405. With respect to claim 5, Yu [PN. 5869873] teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit [Fig. 6, 3], which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad [Fig. 6, Pad 1] and a ground voltage [Vss], so as to discharge the electrostatic charges; and an anti-latch-up circuit [Fig. 6, R and C], which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal respectively coupled to a voltage source [the point of connection for any power supply such as Vcc, ground, or another device may serve as a pad], the ground voltage [Fig 6, Vss], and the third connection

terminal [Fig. 6, the connection between the R and C elements] of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing the latch-up of the ESD protection circuit; wherein the SCR circuit [Fig. 5] comprises a P-type substrate [Fig. 5, 5]; an N well [Fig. 5, 50], formed in the p-type substrate; a first P+ doped region [Fig. 5, 56], formed in the P-type substrate and coupled to the ground voltage [Vss]; a first N+ doped region [Fig. 5, 54], formed in the P-type substrate, adjacent to the first P+ doped region [Fig. 5, 56], and coupled to the ground voltage [Vss]; a second N+ doped region [Fig. 5, 53], formed between the P-type substrate [5] and the N well [50], adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit; a second P+ doped region [Fig. 5, 52], formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad [Pad 1]; and a third N+ doped region [Fig. 5, 57], formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source [the point of connection for any power supply such as Vcc, ground, or another device may serve as a pad].

However, Yu does not disclose that the anti-latch-up circuit comprises a PMOS transistor, having a gate electrode, a source region coupled to the voltage source, and a drain region coupled to the second N+ doped region; a resistor, having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and a capacitor, having a first

contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor.

Yu [6031405] teaches an electrostatic discharge protection circuit that is immune to latch-up during normal operation. The ESD protection circuit [Fig. 4] comprises an anti-latch-up circuit [Fig. 4, 30] that comprises a PMOS transistor, having a gate electrode, a source region coupled to the voltage source [Fig. 4, source of PMOS transistor [Fig. 4, M1] is coupled to node 11 which is powered from a voltage source connected to IC pad 1], and a drain region coupled to the second N+ doped region; a resistor [Fig. 4, R1], having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor [M1] and the ground voltage; and a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor. [Reversing the positions of latch 30 and SCR 20 in Fig. 4 yields applicant's anti-latch-up circuit 6A]. Furthermore, Yu discloses the claimed invention except for connection between SCR 20 and anti-latch circuit 30 are interchanged with respect to their point of connection to IC pad 1 and ground. It would have been obvious to one having ordinary skill in the art at the time the invention was made to reverse the positions of latch 30 and SCR 20 in Fig. 4, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. In re Einstein, 8 USPQ 167.

Both teaching are related by being electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time

the invention was to combine the teachings of Yu [PN. 6031405], which teaches an anti-latch-up circuit, with the ESD protection circuit of Yu [PN. 5869873] for the benefit of improving the protection capabilities of the device.

3. Claims 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, Patent No. 5,869,873, in view of Chen, Publication No. US2001/0007521A1. With respect to claim 6, Yu [PN. 5869873] teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit [Fig. 6, 3], which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad [Fig. 6, Pad 1] and a ground voltage e [Vss], so as to discharge the electrostatic charges; and an anti-latch-up circuit [Fig. 6, R and C], which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal respectively coupled to a voltage source [the point of connection for any power supply such as Vcc, ground, or another device may serve as a pad], the ground voltage [Fig 6, Vss], and the third connection terminal [Fig. 6, the connection between the R and C elements] of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing the latch-up of the ESD protection circuit; wherein the SCR circuit [Fig. 5] comprises a P-type substrate [Fig. 5, 5]; an N well [Fig. 5, 50], formed in the p-type substrate; a first P+ doped region [Fig. 5, 56], formed in the

P-type substrate and coupled to the ground voltage [Vss]; a first N+ doped region [Fig. 5, 54], formed in the P-type substrate, adjacent to the first P+ doped region [Fig. 5, 56], and coupled to the ground voltage [Vss]; a second N+ doped region [Fig. 5, 53], formed between the P-type substrate [5] and the N well [50], adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit, a second P+ doped region [Fig. 5, 52], formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad [Pad 1]; and a third N+ doped region [Fig. 5, 57], formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source [the point of connection for any power supply such as Vcc, ground, or another device may serve as a pad].

However, Yu does not teach an additional NMOS transistor with a source/drain region and a gate is formed between the first N+ doped region and the second N+ doped region.

Chen teaches an ESD protection circuit with high triggering discharge providing good ESD protection and avoiding the latch up effect. The ESD circuit [Fig. 12A] teaches a second N+ doped region [58], formed between the P-type substrate [42] and the N well [n-well], adjacent to the first N+ doped region [48], and coupled to the sixth connection terminal of the anti-latch-up circuit, wherein an additional NMOS transistor [Fig. 12A, first N+ doped region 48, second N+ doped region 58 and a gate 62 constitute the drain, source and gate of the NMOS transistor, Paragraph No. 48, lines 13-16] with a source/drain region and

a gate is formed between the first N+ doped region [48] and the second N+ doped region [58].

Both teachings are related by being electrostatic discharge protection circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen, which teaches an additional NMOS transistor between the first N+ doped regin and the second N+ doped region, with the ESD protection circuit of Yu in order to provide an ESD protection circuit with high triggering current, having the advantages of low holding voltage.

With respect to claims 8 and 11, Yu [PN. 5869873] teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit [Fig. 6, 3], which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad [Fig. 6, Pad 1] and a ground voltage [Vss], so as to discharge the electrostatic charges; and an anti-latch-up circuit [Fig. 6, R and C], which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal respectively coupled to a voltage source [the point of connection for any power supply such as Vcc, ground, or another device may serve as a pad], the ground voltage [Fig 6, Vss], and the third connection terminal [Fig. 6, the connection between the R and C elements] of the SCR circuit, whereby an anti-latch-up signal is sent from the

sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing the latch-up of the ESD protection circuit;

However, Yu does not disclose that the SCR circuit comprises a P-type substrate, an N well, a first P+, a first N+, a second P+, a third P+, and a second N+ doped regions. Yu also does not disclose an additional PMOS transistor with a source/drain region and a gate electrode of the p-type LVTSCR circuit is formed between the second P+ doped region and the third P+ doped region.

Chen teaches an ESD protection circuit with high triggering discharge providing good ESD protection and avoiding the latch up effect. The SCR circuit [Fig. 13C] comprises a P-type substrate [42]; an N well [n-well] formed in he p-type substrate; a first P+ doped region [52], formed in the P-type substrate and coupled to the ground voltage [Vss]; a first N+ doped region [48], formed in he P-type substrate, adjacent to the first P+ doped region; a second P+ doped region [78], formed between the P-type substrate and the N well, adjacent to the first N+ doped region; a third P+ doped region [46], formed in the N well, adjacent to the second P+ doped region, and coupled to the I/O pad [Node 40], wherein an additional PMOS transistor [Fig. 13C, a second P+ doped region 78, a third P+ doped region 46 and a gate 72 constitute the drain, source and gate of the PMOS transistor, Paragraph No. 50, lines 14-18]; and a second N+ doped region [50], formed in the N well, adjacent to the third P+ doped region, and coupled to the I/O pad [Node 40].

With respect to claim 9, Yu [PN. 5869873] teaches an anti-latch-up circuit [Fig. 6] that comprises a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source [the point of connection for any power supply such as VDD, ground, or another device may serve as a pad]; and a resistor, having a first end and a second end, respectively coupled to the second P+ doped region and the ground voltage.

With respect to claim 10, Yu [PN. 5869873] teaches an anti-latch-up circuit [Fig. 6, NMOS transistor, R,C] that comprises an NMOS transistor, having a gate electrode, a source region coupled to the ground voltage [Vss], and a drain region coupled to the second P+ doped region; a capacitor [C], having a first contact end and a second contact end, respectively coupled to the gate electrode of the NMOS transistor and the ground voltage; and a resistor [R], having a first end and a second end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor. [Reversing the positions of R and C in Fig. 6 yields applicant's anti-latch-up circuit]. Furthermore, Yu discloses the claimed invention except for connection between R and C are interchanged with respect to their point of connection to IC pad 1 and ground. It would have been obvious to one having ordinary skill in the art at the time the invention was made to reverse the positions of R and C, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. In re Einstein, 8 USPQ 167.

Allowable Subject Matter

4. Claims 7 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 7: Yu [PN. 6031405] teaches an anti-latch-up circuit that comprises a PMOS transistor, a resistor, and a capacitor, but does not disclose that the gate electrode of the additional NMOS transistor of the LVTSCR circuit is also coupled to the gate electrode o the PMOS transistor. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 12: Yu [PN. 5869873] teaches an anti-latch-up circuit [Fig. 6] that comprises an NMOS transistor, a capacitor and a resistor, but does not disclose that the gate electrode of the additional PMOS transistor of the p-type LVTSCR circuit is also coupled to the gate electrode of the NMOS transistor. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

5. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
01/05/2006

PHUONG T. VU
PRIMARY EXAMINER